**IN THE DRAWINGS:**

The attached sheet of drawings includes changes to FIG. 11. This sheet, which includes FIGS. 6-11, replaces the previous drawing sheet including FIGS. 6-11. In FIG. 11, the solder balls are shown as being connected to at least one signal and at least connected to the voltage reference signal, as suggested by the Examiner. (See attached Replacement Sheet and Annotated Sheet Showing Changes.)

## REMARKS

The Office Action mailed January 4, 2006, has been received and reviewed. Claims 24 through 26, and 28 through 31, are currently pending in the application. Claims 24 through 26, and 28 through 31, stand rejected. Applicant respectfully requests reconsideration of the application with respect to the analysis presented herein.

### Objections to Drawings

Fig. 11 has been modified to show the solder balls being connected to at least one signal and at least connected to the voltage reference signal, as suggested by the Examiner.

### Objections to Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter.

The Examiner states that:

> "[t]he specification needs to provide an explicit description with respect to the FIG. 11 embodiment of the connection of the solder balls to at least one signal trace and the voltage reference signal as recited in amended claims 24 and 31. Since this amended limitation is considered not to be "new matter," then an amendment to the fig. 11 adding the amended claim limitation would be appropriate."

Appropriate amendments have been made to paragraph 0032 describing the connection to the solder balls.

### 35 U.S.C. § 112 Claim Rejections

Claims 24 through 26, 28 through 31, stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The Examiner states that:

> "[i]t appears that the reference to the "semiconductor substrate" and "solder balls" relates to the embodiment depicted and describe relative to "figure 11", while the reference to the slotted voltage reference plane and isolated signal traces relate to the embodiment of "figure 13". However, there does not appear to be any disclosure in the original specification as to an embodiment combining the "semiconductor substrate/solder balls embodiment of "figure 11" with the slotted voltage reference plane/isolated signal traces embodiment of "figure 13"."

Applicants disagree with the Examiner's characterization that figure 11 and figure 13 necessarily represent different embodiments. In describing Fig. 13, the specification states at the second sentence of paragraph 0034 that "[a]s shown in Figure 13, a layer of conductive material on a **substrate** 32 has been removed only around the coplanar signal traces 38. Methods of removing selected portions of conductive material from a substrate, such as by masking and etching, are well known in the art."

Furthermore, in describing Fig. 11, the specification, prior to the amendment herein, states that "Figure 11 illustrates an embodiment of the present invention wherein circuit traces 24 are placed on the surface of a **semiconductor substrate** 26, more particularly, in a flip-chip ball grid array ("BGA") application. Like previous embodiments, the circuit traces 24 are configured such that a voltage reference trace is placed between each of two signal traces so that no signal trace is placed immediately adjacent another signal trace."

However, the specification generally refers to a substrate as a generic term encompassing different forms of substrate. For example, paragraph 0027 of the specification states "[a]s used herein, the term "circuit trace" refers not only to a surface conductive path which is conventionally formed upon the surface of a printed circuit board, but to any conductive path formed on, in or through **a substrate such as a printed circuit board, thin film device or other semiconductor device.**" Similarly, at paragraph 0035, the specification states that "[f]igure 14 is a block diagram of an electronic system 100 which includes components having one or more **printed circuit boards ("PCB") 106 or other substrates** comprising circuit traces configured according to one or more embodiments of the present invention." Finally, at paragraph 0036, the specification states that "[a]s shown in Figure 15, **circuit traces 118 may be fabricated on the surface of a semiconductor wafer** 116 of silicon, gallium arsenide, or indium phosphide in accordance with one or more embodiments of the present invention."

The specification, in its discussion of Fig. 13 describes a "substrate." It is clear, therefore, that the embodiment illustrated in Fig. 13 may be applied to any of the recited substrates, and their equivalents. Therefore, Fig. 13, and the description of Fig. 13 is applicable to the embodiment of Fig. 11 including solder balls and a semiconductor substrate as is found in a ball grid array.

Claims 28 through 30, stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The Examiner states that:

> "it is unclear whether the recited "electrically insulative layer" can properly depend from or properly further limit a "substrate" which has been previously defined as being a "semiconductor". That is to say, a "semiconductor" has material properties which are materially different from that of "an electrically insulative layer" and as such would appear incompatible with it's use as a "semiconductor substrate." Clarification is needed."

In clarification, Applicant points out that a portion of claim 28 recites "wherein the semiconductor substrate includes: an electrically insulative layer **disposed on** the electrically conductive layer; and an additional electrically conductive layer disposed on the electrically insulative layer." As a consequence, the electrically insulative layer is not necessarily part of the "bare" semiconductor substrate, as the Examiner seems to be implying. Rather, the electrically insulative layer is **disposed on** the semiconductor substrate, with a material such as an oxide or passivation layer, to create a semiconductor substrate with multiple routing layers as is commonly know by those of ordinary skill in the art.

Claims 29 and 30 depend from claim 28 and, therefore, include the same element of "an electrically insulative layer **disposed on** the electrically conductive layer."

**35 U.S.C. § 103(a) Obviousness Rejections**

Obviousness Rejection Based on U.S. Patent No. 6,181,278 to Kakimoto et al. in view of U.S. Patent No. 5,796,321 to Caillat et al.

Claims 24 and 26, stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kakimoto et al. (U.S. Patent No. 6,181,278) in view of Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Regarding claim 24, in rejecting claim 24 the Examiner states, in part, that:

> "Kakimoto et al discloses in fig. 21 thereof, a ground and signal trace pattern configuration disposed on a surface of a semiconductor substrate (20). Note that the pattern comprises a voltage reference or ground plane (210) substantially surrounding the surface of the semiconductor substrate and patterned to include slots therein."

However, the Examiner has not addressed the element as recited in claim 24 of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots." Even if one considers the conductive trace connected to element 37a in FIG. 21 a signal trace, which is not entirely clear from the figure or the detailed description, there is not a voltage reference plane that provides a **continuous electrical connection** around the conductive trace connected to element 37a. Rather, there appears to be eight different segments surrounding most of the conductive trace connected to element 37a. Therefore, these eight different segments, by themselves do not form a voltage reference plane

that provides a **continuous electrical connection** around the conductive trace, as is recited in claim 24. Instead, it appears to Applicant, that these eight different segments are separate conductive traces of a possible voltage reference plane, if they are connected together.

Applicant recognizes that in discussing FIG. 21, Kakimoto et al. apparently describe external methods of connecting these eight different segments together to "attain a same potential" (col. 13, line 44). However, this requires additional elements, not recited in claim 24, to operably couple the eight different segments together.

Furthermore, Applicant can find no teaching or suggestion in the Caillat reference to the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," as is recited in claim 24.

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 24 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Kakimoto et al. in view of Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 24 be withdrawn.

Regarding claim 26, Applicant submits that claim 26 is allowable, at least by virtue of its dependency from allowable base claim 24. Applicant, therefore, respectfully requests reconsideration and allowance of claim 26.

Obviousness Rejection Based on U.S. Patent No. 6,175,287 to Lampen et al in view of U.S. Patent No. 5,796,321 to Caillat et al.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lampen et al. (U.S. Patent No. 6,175,287) in view of Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 24, in rejecting claim 24 the Examiner states, in part, that:

> "Lampen et al in fig. 6 discloses a semiconductive MMIC having a ground or voltage reference plane (68) disposed over substantially the entire surface of the MMIC. Moreover, note that the ground plane includes a plurality of slots (72)

disposed therein in which respective short conductive traces or pads (70) are disposed. Furthermore, note that the traces are disposed such that the ground plane electrically isolates adjacent conductive traces."

However, as with the rejection discussed above concerning Kakimoto et al., the Examiner has not addressed the element as recited in claim 24 of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots." FIG. 6 of the Lampen reference does not show, nor can Applicants find any description in the specification of the ground plane 68 forming a continuous electrical connection around the conductive traces or pads (70).

Furthermore, Applicant can find no teaching or suggestion in the Caillat reference to the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," as is recited in claim 24.

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 24 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Lampen et al. in view of Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 24 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 6,181,278 to Kakimoto et al. and/or U.S. Patent No. 6,175,287 to Lampen et al. in view of U.S. Patent No. 5,796,321 to Caillat et al. and further in view of U.S. Patent No. 5,631,446 to Quan

Claim 25, stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kakimoto et al. (U.S. Patent No. 6,181,278) and/or Lampen et al. (U.S. Patent No. 6,175,287) in view of Caillat et al. (U.S. Patent No. 5,796,321), and further in view of Quan (U.S. Patent No. 5,631,446). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 25, Applicant submits that claim 25 is allowable, at least by virtue of its dependency from allowable base claim 24. Applicant, therefore, respectfully requests reconsideration and allowance of claim 25.

Obviousness Rejection Based on U.S. Patent No. 6,373,740 to Forbes et al. in view of either U.S Patent No. 6,181,278 to Kakimoto et al., U.S. Patent No. 6,232,660 to Kakimoto et al. or U.S. Patent No. 6,175,287 to Lampen et al., as modified by U.S. Patent No. 5,796,321 to Caillat et al.

Claim 31 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Forbes (U.S. Patent No. 6,373,740) in view of either Kakimoto et al. (U.S. Patent No. 6,232,660), Kakimoto et al. (U.S. Patent No. 6,175,287), or Lampen et al. (U.S. Patent No. 6,175,287), as modified by Caillat et al. (U.S. Patent No. 5,796,321). Applicant respectfully traverses this rejection, as hereinafter set forth.

Regarding claim 31, claim 31 includes all of the subject matter of independent claim 24. Therefore, the analysis presented above for the obviousness rejection of claim 24 with respect to Kakimoto et al. ('278) in view of Caillat et al. and the obviousness rejection of claim 24 with respect to Lampen et al. in view of Caillat et al. are equally applicable to claim 31.

In addition, as stated by the Examiner, "Forbes discloses an electronic system including a processor, memory device, input device, output device, data storage device, etc, but does not disclose such devices being semiconductor substrates having the recited conductive patterns connected by solder balls." Finally, Applicant can find no description in the Kakimoto et al.'660 reference of the element recited in claim 31 of, "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots."

Therefore, Applicant asserts that the 35 U.S.C. § 103(a) rejection of claim 31 is improper because the element of "wherein the voltage reference plane provides a **continuous electrical connection** around each of the plurality of signal trace slots," is not taught or suggested by the combination of Forbes et al. in view of either Kakimoto et al. '660 or Kakimoto et al. '287 or Lampen et al., as modified by Caillat et al. As a result, Applicant respectfully requests that the rejection of claim 31 be withdrawn.

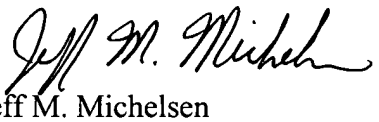
## ENTRY OF AMENDMENTS

The amendments to the specification and drawings above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

## CONCLUSION

Claims 24-26 and 28-31 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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Date: April 4, 2006
JMM/sfc:eg
Document in ProLaw

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PATENT & TRADEMARK OFFICE

TITLE: METHOD AND APPARATUS OF INTERPOSING VOLTAGE REFERENCE TRACES BETWEEN SIGNAL TRACES IN SEMICONDUCTOR DEVICES
Serial No.: 09/548,942
Docket No.: 2269-4161US
**ANNOTATED SHEET SHOWING CHANGES**

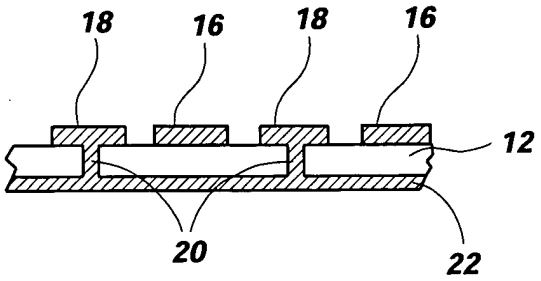


Fig. 6

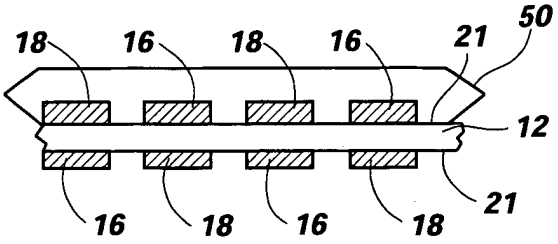


Fig. 8

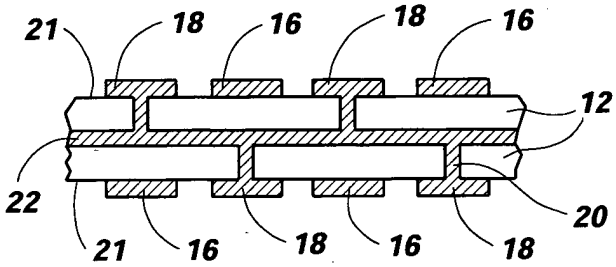


Fig. 7

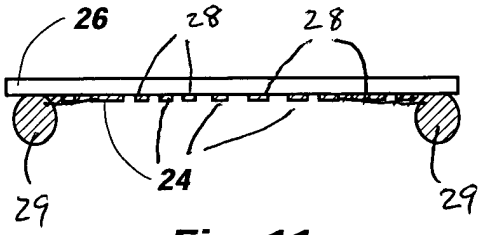


Fig. 11

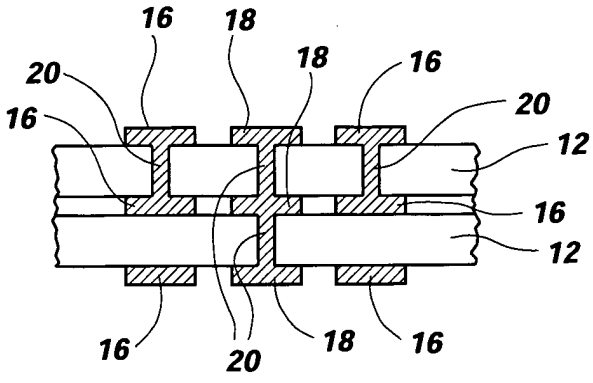


Fig. 10

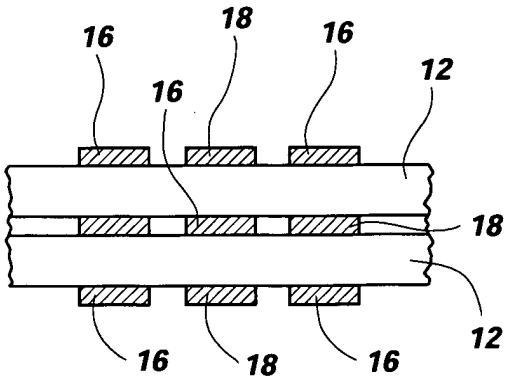


Fig. 9